

PATENT COOPERATION TREATY

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INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY

(Chapter II of the Patent Cooperation Treaty)

(PCT Article 36 and Rule 70)

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Applicant's or agent's file reference M04-TJ003CT1	FOR FURTHER ACTION		See Form PCT/IPEA/416
International application No. PCT/JP2004/003808	International filing date (day/month/year) 19.03.2004	Priority date (day/month/year) 20.03.2003	
International Patent Classification (IPC) or national classification and IPC H01L21/336			
Applicant MATSUSHITA ELECTRIC INDUSTRIAL CO. LTD et al.			

1. This report is the international preliminary examination report, established by this International Preliminary Examining Authority under Article 35 and transmitted to the applicant according to Article 36.
2. This REPORT consists of a total of 9 sheets, including this cover sheet.
3. This report is also accompanied by ANNEXES, comprising:
 - a. ☒ sent to the applicant and to the International Bureau a total of 5 sheets, as follows:
 - ☒ sheets of the description, claims and/or drawings which have been amended and are the basis of this report and/or sheets containing rectifications authorized by this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions).
 - ☒ sheets which supersede earlier sheets, but which this Authority considers contain an amendment that goes beyond the disclosure in the international application as filed, as indicated in item 4 of Box No. I and the Supplemental Box.
 - b. ☐ (sent to the International Bureau only) a total of (indicate type and number of electronic carrier(s)) , containing a sequence listing and/or tables related thereto, in computer readable form only, as indicated in the Supplemental Box Relating to Sequence Listing (see Section 802 of the Administrative Instructions).

4. This report contains Indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☒ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☒ Box No. VIII Certain observations on the international application

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**INTERNATIONAL PRELIMINARY REPORT
ON PATENTABILITY**

International application No.
PCT/JP2004/003808

Box No. I Basis of the report

1. With regard to the **language**, this report is based on the international application in the language in which it was filed, unless otherwise indicated under this item.
- ☐ This report is based on translations from the original language into the following language , which is the language of a translation furnished for the purposes of:
- ☐ international search (under Rules 12.3 and 23.1(b))
 - ☐ publication of the international application (under Rule 12.4)
 - ☐ international preliminary examination (under Rules 55.2 and/or 55.3)
2. With regard to the **elements*** of the international application, this report is based on *(replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report)*:

Description, Pages

1-25 as originally filed

Claims, Numbers

1-11 received on 06.08.2004 with letter of 03.08.2004

Drawings, Sheets

1/21-21/21 as originally filed

- ☐ a sequence listing and/or any related table(s) - see Supplemental Box Relating to Sequence Listing
3. ☐ The amendments have resulted in the cancellation of:
- ☐ the description, pages
 - ☐ the claims, Nos.
 - ☐ the drawings, sheets/figs
 - ☐ the sequence listing (*specify*):
 - ☐ any table(s) related to sequence listing (*specify*):
4. ☒ This report has been established as if (some of) the amendments annexed to this report and listed below had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).
- ☐ the description, pages
 - ☒ the claims, Nos. 9-11
 - ☐ the drawings, sheets/figs
 - ☐ the sequence listing (*specify*):
 - ☐ any table(s) related to sequence listing (*specify*):

* If item 4 applies, some or all of these sheets may be marked "superseded."

**INTERNATIONAL PRELIMINARY REPORT
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Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability

1. The questions whether the claimed invention appears to be novel, to involve an inventive step (to be non-obvious), or to be industrially applicable have not been examined in respect of:
- ☐ the entire international application,
 - ☒ claims Nos. 5
- because:
- ☐ the said international application, or the said claims Nos. relate to the following subject matter which does not require an international preliminary examination (specify):
 - ☒ the description, claims or drawings (*indicate particular elements below*) or said claims Nos. 5 are so unclear that no meaningful opinion could be formed (*specify*):
see separate sheet
 - ☐ the claims, or said claims Nos. are so inadequately supported by the description that no meaningful opinion could be formed.
 - ☒ no international search report has been established for the said claims Nos. 5
 - ☐ the nucleotide and/or amino acid sequence listing does not comply with the standard provided for in Annex C of the Administrative Instructions in that:
 - the written form ☐ has not been furnished
 - ☐ does not comply with the standard
 - the computer readable form ☐ has not been furnished
 - ☐ does not comply with the standard
 - ☐ the tables related to the nucleotide and/or amino acid sequence listing, if in computer readable form only, do not comply with the technical requirements provided for in Annex C-*bis* of the Administrative Instructions.
 - ☒ See separate sheet for further details

**INTERNATIONAL PRELIMINARY REPORT
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Box No. V Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes: Claims	6,7,8
	No: Claims	1,2,3,4,9-11
Inventive step (IS)	Yes: Claims	
	No: Claims	1-4, 6-11
Industrial applicability (IA)	Yes: Claims	1-4,6-11
	No: Claims	

2. Citations and explanations (Rule 70.7):

see separate sheet

Box No. VIII Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:

see separate sheet

Re Item I

Basis for the opinion

The amendments filed with the International Bureau under **Article 19(1)** introduce subject-matter which extends beyond the content of the application as filed, contrary to **Article 19(2) PCT**. The amendments concerned are the following:

Claim 9: added method steps (b) "forming an insulating film on the side wall of the trench" and (d) "removing the insulating film"

According to page 15, line 13-17 and page 16, line 2-5, line 13-17, the insulating film consists of a two layer film (4) and (5), from which only one layer (5) is removed and the layer (4) directly on the side wall of the trench remains. Moreover, according to fig. 6 (c), part of the insulating film (5) remains due to the masking effect of the overlying resist mask. Therefore no basis for removing an insulating film that has been formed on the sidewall of the trench can be derived from those passages.

In the second embodiment, the first insulating film (53) is formed on the side wall of the trench. According to page 22, line 14-18, only part of the first insulating film (53) are removed. Therefore also no basis for removing an insulating film can be derived from this passage.

This report is established as if those amendments had not been made.

Re Item III

Non-establishment of opinion with regard to novelty, inventive step and industrial applicability

It is not clear from **claim 5** or from the relevant passages of the description, which surface of the FIN is formed to have a convex shape and how this convex form is to be achieved. Therefore no comparison with the prior art is possible. This claim has been excluded from search and therefore no opinion can be given on this claim.

Re Item V

**Reasoned statement with regard to novelty, inventive step or industrial applicability;
citations and explanations supporting such statement**

Reference is made to the following documents:

- D1:** US-A-4 996 574 (SHIRASAKI MASAHIRO) 26 February 1991 (1991-02-26)
- D2:** EP-A-0 623 963 (SIEMENS AG) 9 November 1994 (1994-11-09)
- D3:** US 2002/003256 A1 (MAEGAWA SHIGETO) 10 January 2002 (2002-01-10)
- D4:** US-B1-6 288 431 (IWASA SHOICHI ET AL) 11 September 2001 (2001-09-11)

1. Independent Claims

1.1 Novelty

The present application does not meet the criteria of **Article 33(1) PCT**, because the subject-matter of **claims 1 and 9** is not new in the sense of **Article 33(2) PCT**.

1.1.1 The document **D2** (whole document) discloses (the references in parentheses applying to this document):

- a semiconductor device comprising:
- a semiconductor substrate (1,2,3) in which a trench is formed;
- a source region (7) and a drain region (7), each of which is buried in the trench and containing an impurity of the same conductive type;
- a semiconductor FIN (4) buried in the trench and provided between the source region and the drain region;
- a gate insulating film (6) provided on a side surface of the semiconductor FIN as well as an upper surface of the semiconductor FIN; and
- a gate electrode (5) having two end portions each of which protrudes downward in the trench so as to extend along the gate insulating film on the semiconductor FIN and formed on the gate insulation film, **which is relevant to claim 1.**

1.1.2 The document **D1** (column 7, line 34 - column 8, line 15; claims 11-13; figures 10, 11) discloses (the references in parentheses applying to this document):

a method for fabricating a semiconductor device, the device including a semiconductor substrate (32) in which a trench (30) is formed, a source region (31a) and a drain region (31b), each of which is buried in the trench and containing an impurity of the same conductive type, a semiconductor FIN (31c) buried in the trench and provided between the source region and the drain region, a gate insulating film (34) provided on a side surface of the semiconductor FIN as well as an upper surface of the semiconductor FIN; and a gate electrode (35) provided on the gate insulation film, the method comprising the steps of:

- (a) forming a trench in the semiconductor substrate
- (c) forming a semiconductor layer in the trench formed in the semiconductor substrate;
- (e) forming a gate insulating film on an upper surface part of the semiconductor layer which is to be a semiconductor FIN as well as a side surface of the part of the semiconductor layer;
- (f) forming a gate electrode on the gate insulating film; and
- (g) introducing an impurity into the semiconductor layer, using the gate electrode as a mask, to form a source region and a drain region in regions of the semiconductor layer located on sides of and under the gate electrode, respectively, and then forming a semiconductor FIN in a region of the semiconductor layer interposed between the source region and the drain region and located directly under the gate electrode, **which is relevant to claim 9.**

1.1.3 Moreover, it should also be pointed out that **claim 1 and 9** are also **not new** over the disclosure of document **D1** (column 7, line 34 - column 8, line 15; claims 11-13; figures 10, 11), **D3** (page 6, paragraph 89 - 94; page 7, paragraph 100 - page 9, paragraph 123; claims; figures 1-23), **D4** (column 1, line 66 - column 2, line 34; column 3, line 35 - column 4, line 26; column 11, line 40 - column 13, line 58; column 18, line 42 - column 20, line 46; claims; figures 1-6)

1.2 Inventive Step

The present application does not meet the criteria of **Article 33(1) PCT**, because the subject-matter of **claim 6** does not involve an inventive step in the sense of **Article 33(3)**

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1.2.1 The document **D2** (whole document) is regarded as being the closest prior art to the subject-matter of **claim 6**, and discloses (the references in parentheses applying to this document):

a semiconductor device comprising:

a first field effect transistor including a semiconductor substrate (1,2,3) in which a trench is formed, a first source region (7) and a first drain region (7), each of which is buried in the trench and containing an impurity of the same conductive type, a semiconductor FIN (4) buried in the trench and provided between the first source region and the first drain region, a first gate insulating film (6) provided on a side surface of the semiconductor FIN as well as an upper surface of the semiconductor FIN, and
a first gate electrode (5) having two end portions each of which protrudes downward in the trench so as to extend along the gate insulating film on the semiconductor FIN and formed on the gate insulation film.

The subject-matter of **claim 6** therefore differs from this known semiconductor device in that a second field effect transistor is included.

The problem to be solved by the present invention may therefore be regarded as to use the first field effect transistor in an integrated circuit.

The document **D2** suggests the integration of the disclosed semiconductor device together with other semiconductor devices. The skilled person would therefore readily integrate the device with other MOSFET or even with devices of the same kind, thereby arriving at the subject matter of **claim 6**.

1.2.2 Moreover, **claim 6** is also not considered as involving an inventive step over the disclosure of document **D1** (column 7, line 34 - column 8, line 15; claims 11-13; figures 10, 11), **D3** (page 6, paragraph 89 - 94; page 7, paragraph 100 - page 9, paragraph 123; claims; figures 1-23), **D4** (column 1, line 66 - column 2, line 34; column 3, line 35 - column 4, line 26; column 11, line 40 - column 13, line 58; column 18, line 42 - column 20, line 46; claims; figures 1-6) as the integration of several semiconductor devices is common in the

art and would be employed by the skilled person in accordance with circumstances without the exercise of inventive skill.

2. Dependent Claims

2.1 Novelty / Inventive Step

Dependent **claims 2 - 4, 7 - 8 and 10 - 11** do not contain any features which, in combination with the features of any claim to which they refer, meet the requirements of the PCT in respect of novelty or inventive step for the following reasons:

The use of Si as the FIN-material is disclosed in document **D1**. Furthermore the use of SiGe or SiGeC is well known in the art, **which is relevant to claim 2**.

The features of **claims 3, 4, 7 and 8** are disclosed in document **D1**.

The steps of **claim 10** are disclosed in document **D3** (page 8, paragraph 116; fig 18).

The steps of **claim 11** are disclosed in document **D1** (column 7, line 53 - 63; fig 10).

Re Item VIII

Certain observations on the international application

The application does not meet the requirements of **Article 6 PCT**, because **claims 1 and 6** is not clear.

Although **claim 6** has been formulated as an independent claim, it contains all the features of **claim 1** and therefore is considered a dependent claim. The aforementioned claims therefore lack conciseness and as such do not meet the requirements of **Article 6 PCT**.

CLAIMS

1. (Amended) A semiconductor device comprising:

a semiconductor substrate in which a trench is formed;

a source region and a drain region, each of which is buried in the trench and
5 contains an impurity of the same conductive type;

a semiconductor FIN buried in the trench and provided between the source region
and the drain region;

a gate insulating film provided on a side surface of the semiconductor FIN as well
as an upper surface of the semiconductor FIN; and

10 a gate electrode having two end portions each of which protrudes downward in the
trench so as to extend along the gate insulating film on the semiconductor FIN and formed
on the gate insulating film.

2. The semiconductor device of claim 1, wherein the semiconductor FIN is made
15 of one material selected from the group consisting of Si, $\text{Si}_{1-x}\text{Ge}_x$ ($0 < x \leq 1$), and $\text{Si}_{1-y-z}\text{Ge}_y\text{C}_z$ ($0 < y < 1$, $0 < z < 1$, $0 < y + z < 1$).

3. The semiconductor device of claim 1, wherein the gate electrode is provided on
the gate insulating film so as to extend over the semiconductor substrate,

20 wherein an isolation insulating film is further provided between part of the
semiconductor substrate located in a side wall portion of the trench and part of the gate
electrode located over the side wall of the semiconductor FIN; and

wherein an insulating film is further provided between part of the semiconductor
substrate in which the trench is not formed and the gate electrode.

4. The semiconductor device of claim 1, wherein the gate electrode is provided on the gate insulating film so as to extend over the semiconductor substrate,

wherein the gate insulating film is provided on the side and upper surfaces of the semiconductor FIN as well as part of the semiconductor substrate in which the trench is not formed, and

wherein part of the gate insulating film located on the part of the semiconductor substrate in which the trench is not formed is interposed between the semiconductor substrate and the gate electrode.

5. The semiconductor device of any one of claims 1 through 4, wherein the semiconductor FIN is formed so as to have a convex shape when viewed from the bottom of the trench.

6. (Amended) A semiconductor device comprising:

a first field-effect transistor including a semiconductor substrate in which a trench is formed, a first source region and a first drain region each of which is buried in the trench and contains an impurity of the same conductive type, a semiconductor FIN buried in the trench and provided between the first source region and the first drain region, a first gate insulating film provided on a side surface of the semiconductor FIN as well as an upper surface of the semiconductor FIN, and a first gate electrode having two end portions each of which protrudes downward in the trench so as to extend along the gate insulating film on the semiconductor FIN and formed on the gate insulating film; and

a second field-effect transistor including a second gate insulating film provided on the semiconductor substrate, a second gate electrode provided on the second gate insulating film, and second source and drain regions each of which contains an impurity

and is provided in a region of the semiconductor substrate located on a side of and under the second gate electrode.

7. The semiconductor device of claim 6, wherein the first gate electrode is provided on the first gate insulating film so as to extend over the semiconductor substrate, and

wherein the first field-effect transistor further includes an isolation insulating film formed between part of the semiconductor substrate located in a side wall portion of the trench and part of the first gate electrode provided over the side surface of the semiconductor FIN and a second insulating film formed between the semiconductor substrate and the first gate electrode.

8. The semiconductor device of claim 6, wherein the first gate electrode is provided on the first gate insulating film so as to extend over the semiconductor substrate,

wherein the first gate insulating film is provided on the side and upper surfaces of the semiconductor FIN as well as part of the semiconductor substrate in which the trench is not formed, and

wherein part of the gate insulating film located on the part of the semiconductor substrate in which the trench is not formed is interposed between the semiconductor substrate and the first gate electrode.

9. (Amended) A method for fabricating a semiconductor device, the device including a semiconductor substrate in which a trench is formed, a source region and a drain region each of which is buried in the trench and contains an impurity of the same conductive type, a semiconductor FIN buried in the trench and provided between the

source and drain regions, a gate insulating film provided on a side surface of the semiconductor FIN as well as an upper surface of the semiconductor FIN, and a gate electrode formed on the gate insulating film, the method comprising steps of:

(a) forming the trench in the semiconductor substrate;

5 (b) forming an insulating film on a side wall of the trench;

(c) forming a semiconductor layer including the semiconductor FIN in the trench using the insulating film as a mask;

(d) removing the insulating film;

(e) forming a gate insulating film on an upper surface of part of the semiconductor layer which is to be the semiconductor FIN as well as a side surface of the part of the semiconductor layer;

(f) forming a gate electrode on the gate insulating film; and

(g) introducing an impurity into the semiconductor layer, using the gate electrode as a mask, to form a source region and a drain region in regions of the semiconductor layer located on sides of and under the gate electrode, respectively, and then forming a semiconductor FIN in a region of the semiconductor layer interposed between the source region and the drain region and located directly under the gate electrode.

10. (Amended) The method for fabricating a semiconductor device of claim 9, wherein in the process step (f), the gate electrode is provided on the gate insulating film so as to extend over the semiconductor substrate, and

wherein the method further includes the step (h) of forming an isolation insulating film in a side wall portion of the trench and the step (i) of forming an insulating film on the semiconductor substrate.

11. (Amended) The method for fabricating a semiconductor device of claim 9, wherein the gate electrode is provided on the gate insulating film so as to extend over the semiconductor substrate,

wherein the gate insulating film formed in the step (e) is provided on side and
5 upper surfaces of part of the semiconductor layer which is to be the semiconductor FIN as well as part of the semiconductor substrate in which the trench is not formed, and

wherein in the step (f), the gate electrode is provided so that the gate insulating film is interposed between the part of the gate electrode and the semiconductor substrate.